WHAT IS CLAIMED IS:

1. A processor comprising:

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal and which do not overlap with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either the first or second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein

when either one of the first and second reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first and second initial setting areas.

2. The processor according to claim 1, further comprising:

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal and which do not overlap with both said

first initial setting area and said second initial setting area; and

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed, wherein

when any one of the first through third reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through third initial setting areas.

3. The processor according to claim 2, wherein

the first initial setting area is formed by a first register group for performing communication between the processor and an outside of the processor,

the third initial setting area is formed by a second register group relating to execution of instructions inside the processor, and

the second initial setting area is an area other than both the first register group and the second register group.

4. The processor according to claim 2, further comprising:

an n-th initial setting area, where n is an integer having value equal to or more than 4, which do not overlap

with each initial setting area from the first initial setting area through an (n-1)-th initial setting area and which is initialized based on an input of the first reset signal through an n-th reset signal different from any of the first through an (n-1)-th reset signal; and

an n-th flag that is cleared by an input of any of the first reset signal through the n-th reset signal and that is set when initial setting of the n-th initial setting area has been completed, wherein

when any one of the first through n-th reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through n-th initial setting areas.

5. The processor according to claim 1, wherein the processor is provided with an external input terminal for receiving the respective reset signals from the outside.

6. The processor according to claim 1, wherein the respective reset signals are generated within the processor.

7. A method of controlling resetting of a processor, the processor including

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal and which do not overlap with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either the first or second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein

when either one of the first and second reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first and second initial setting areas,

the method comprising:

the step in which flags that correspond to each reset signal type are cleared;

the step in which a state of each flag is confirmed, initial setting is performed for an initial setting area corresponding to the cleared flags and, after the initial setting is completed, setting corresponding flags is repeatedly performed until all of the flags are placed in a set state.

8. A method of controlling resetting of a processor, the processor including

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal and which do not overlap with said first initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed; and

a second flag that is cleared by an input of either the first or second reset signals and that is set when initial setting of the second initial setting area has been completed, wherein

when either one of the first and second reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first and second initial setting areas,

the method comprising the steps of:

clearing the first flag if the first reset signal is received, and clearing the first and second flags if the second reset signal is received;

checking which flag/s has/have been cleared out of the first and second flags;

initializing initial setting area/s corresponding to the cleared flag/s out of the first and second areas, and

setting flag/s corresponding to the initial setting area/s which has/have been initialized out of the first and second areas.

9. A method of controlling resetting of a processor, the processor including

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal and which do not overlap with said first initial setting area;

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal and which do not overlap with both said first initial setting area and said second initial setting area;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed;

a second flag that is cleared by an input of either the first or second reset signals and that is set when initial setting of the second initial setting area has been completed,

and

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed, wherein

when any one of the first through third reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through third initial setting areas,

the method comprising the steps of:

clearing the first flag if the first reset signal is received, clearing the first and second flags if the second reset signal is received, and clearing the first through third flags if the third reset signal is received;

checking which flag/s has/have been cleared out of the first through third flags;

initializing initial setting area/s corresponding to the cleared flag/s out of the first through third areas, and

setting flag/s corresponding to the initial setting area/s which has/have been initialized out of the first through third areas.

10. The method of controlling resetting of a processor according to claim 9, wherein

the first initial setting area is formed by a first register group for performing communication between the processor and an outside of the processor,

the third initial setting area is formed by a second register group relating to the execution of instructions inside the processor, and

the second initial setting area is an area other than both the first register group and the second register group.

11. A method of controlling resetting of a processor, the processor including

a first initial setting area which is initialized based on an input of a first reset signal;

a second initial setting area which is initialized based on an input of either the first reset signal or a second reset signal and which do not overlap with said first initial setting area;

a third initial setting area which is initialized based on an input of the first or second reset signals or a third input signal and which do not overlap with both said first initial setting area and said second initial setting area;

an n-th initial setting area, where n is an integer having value equal to or more than 4, which do not overlap with each initial setting area from the first initial setting

area through an (n-1)-th initial setting area and which is initialized based on an input of the first reset signal through an n-th reset signal different from any of the first through an (n-1)-th reset signal;

a first flag that is cleared by an input of the first reset signal and that is set when initial setting of the first initial setting area has been completed;

a second flag that is cleared by an input of either the first or second reset signals and that is set when initial setting of the second initial setting area has been completed;

a third flag that is cleared by an input of any one of the first through third reset signals and that is set when initial setting of the third initial setting area has been completed, and

an n-th flag that is cleared by an input of any of the first reset signal through the n-th reset signal and that is set when initial setting of the n-th initial setting area has been completed, wherein

when any one of the first through n-th reset signals is input, initial setting area/s corresponding to cleared flag/s is/are initialized out of the first through n-th initial setting areas,

the method comprising the steps of:

clearing the first flag if the first reset signal is

received, clearing the first and second flags if the second reset signal is received, clearing the first through third flags if the third reset signal is received, and clearing the first through n-th flags if the n-th reset signal is received;

checking which flag/s has/have been cleared out of the first through n-th flags;

initializing initial setting area/s corresponding to the cleared flag/s out of the first through n-th areas, and

setting flag/s corresponding to the initial setting area/s which has/have been initialized out of the first through n-th areas.